	Type	Hits	Search Text	DBs	Time Stamp
2	BRS	12	circuit same latency same loop and (hdl or vhdl)	USPAT; US-PGPUB	2003/05/08 14:10
3	BRS	7	circuit same latency same loop and (hdl or vhdl)	USPAT; DERWENT	2003/05/08 14:08
4	BRS	64	circuit same delay same loop and (hdl or vhdl)	USPAT; DERWENT	2003/05/08 14:10
5	BRS	10	circuit same delay same loop and (hdl or vhdl) and pipeline	USPAT; DERWENT	2003/05/08 14:11

	Type	Hits	Search Text	DBs	Time Stamp
6	BRS	5	lock same step same consistency same check	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
7	BRS	593	lock same step same controller and code	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
8	BRS	41	lock same step same controller and code and emulator	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
9	BRS	66	lock same step same consistency	USPAT; US-PGPUB; DERWENT	2003/05/12 11:10
10	BRS	24	lock same step same consistency and controller and code	USPAT; US-PGPUB; DERWENT	2003/05/12 14:17
25	BRS	425	latency same delay same pipeline	USPAT; US-PGPUB; DERWENT	2003/05/29 15:49
26	BRS	39	latency same delay same pipeline and initiation	USPAT; US-PGPUB; DERWENT	2003/05/30 09:08

	Comments	Error Definition	Errors
6			0
7			0
8			0
9			0
10			0
25			0
26			0

Citation

European Design Automation Conference >archive
Proceedings of the conference on European design automation conference >toc
1994 , Grenoble, France

A VHDL-based design methodology: the design experience of a high performance ASIC chip

Authors
Maurizio Valle
Daniele Caviglia
Marco Cornero
Giovanni Nateri
Luciano Briozzo

92
144
191
118

Sponsor
SIGDA : ACM Special Interest Group on Design Automation

Publisher
IEEE Computer Society Press Los Alamitos, CA, USA

Pages: 664 - 669 Series-Proceeding-Article
Year of Publication: 1994 – SEPTEMBER
ISBN:0-89791-685-9

INDEX TERMS

Primary Classificati n:
B. Hardware
↳ B.7 INTEGRATED CIRCUITS

Citation

European Design Automation Conference >archive
Proceedings of the conference on European design automation conference >toc
1994 , Grenoble, France

Scheduling of behavioral VHDL by retiming techniques

Authors
N. Wehn
J. Biesenack
Peter Duzy
T. Langmaier
M. Münch
Michael Pilsl
S. Rumler

Sponsor
SIGDA : ACM Special Interest Group on Design Automation

Publisher
IEEE Computer Society Press Los Alamitos, CA, USA

Pages: 546 - 551 Series-Proceeding-Article
Year of Publication: 1994
ISBN:0-89791-685-9

Citation

Annual ACM IEEE Design Automation Conference >archive
Proceedings of the 28th conference on ACM/IEEE design automation conference >toc
1991 , San Francisco, California, United States

Scheduling for functional pipelining and loop winding

Authors
Cheng-Tsung Hwang
Yu-Chin Hsu
Youn-Long Lin

Sponsors
SIGDA : ACM Special Interest Group on Design Automation
IEEE-CS : Computer Society

Publisher
ACM Press New York, NY, USA

Pages: 764 - 769 Series-Proceeding-Article
Year of Publication: 1991
ISBN:0-89791-395-7

http://doi.acm.org/10.1145/127601.127766 (Use this link to Bookmark this page)

Citation

Annual ACM IEEE Design Automation Conference >archive
Proceedings of the 29th ACM/IEEE conference on Design automation conference >toc
1992 , Anaheim, California, United States

High-level synthesis from VHDL with exact timing constraints

Authors
A. Stoll
P. Duzy

Sponsors
EDAC : Electronic Design Automation Consortium
IEEE-CS : Computer Society
IEEE-CAS : Circuits & Systems
SIGDA : ACM Special Interest Group on Design Automation

Publisher
IEEE Computer Society Press Los Alamitos, CA, USA

Pages: 188 - 193 Series-Proceeding-Article
Year of Publication: 1992
ISBN:0-89791-516-X

INDEX TERMS

Primary Classification:
B. Hardware
B.5 REGISTER-TRANSFER-LEVEL IMPLEMENTATION

Citation

Annual ACM IEEE Design Automation Conference >archive
Proceedings of the 28th conference on ACM/IEEE design automation conference >toc
1991 , San Francisco, California, United States

CHOP: A constraint-driven system-level partitioner

Authors
Kayhan Kükçakar
Alice C. Parker

Sponsors
SIGDA : ACM Special Interest Group on Design Automation
IEEE-CS : Computer Society

Publisher
ACM Press New York, NY, USA

Pages: 514 - 519 Series-Proceeding-Article
Year of Publication: 1991
ISBN:0-89791-395-7

doi http://doi.acm.org/10.1145/127601.127724 (Use this link to Bookmark this page)

Your search matched **1** of **942182** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

formal approach to the scheduling problem

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A formal approach to the scheduling problem in high level synthesis**
Hwang, C.-T.; Lee, J.-H.; Hsu, Y.-C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 10 Issue: 4 , Apr 1991
Page(s): 464 -475

[Abstract] [PDF Full-Text (980 KB)] **IEEE JNL**

Your search matched **1** of **942182** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

generating pipelined datapaths using reduction techniques

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Generating pipelined datapaths using reduction techniques to shorten critical paths**
Lobo, D.A.; Pangrle, B.M.;
Design Automation Conference, 1992. EURO-VHDL '92, EURO-DAC '92. European , 7-10 Sep 1992
Page(s): 390 -395

[Abstract] [PDF Full-Text (612 KB)] **IEEE CNF**

Your search matched **1** of **942182** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

chippe: a system for constraint driven behavioral synthesis

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Chippe: a system for constraint driven behavioral synthesis**
Brewer, F.; Gajski, D.D.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 9 Issue: 7 , Jul 1990
Page(s): 681 -695

[Abstract] [PDF Full-Text (1416 KB)] **IEEE JNL**

Your search matched **1** of **942182** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

vhdl as input for high-level synthesis

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **VHDL as input for high-level synthesis**
Camposano, R.; Saunders, L.F.; Tabet, R.M.;
Design & Test of Computers, IEEE , Volume: 8 Issue: 1 , Mar 1991
Page(s): 43 -49

[Abstract] [PDF Full-Text (816 KB)] **IEEE JNL**

Your search matched **1** of **942182** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

asic design using the high-level synthesis system callas

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **ASIC design using the high-level synthesis system CALLAS: a case study**
Koster, M.; Geiger, M.; Duzy, P.;
Computer Design: VLSI in Computers and Processors, 1990. ICCD '90. Proceedings., 1990 IEEE International Conference on , 17-19 Sep 1990
Page(s): 141 -146

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

Your search matched **1** of **942182** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

lower bounds on the iteration time and the number of resources

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Lower bounds on the iteration time and the number of resources for functional pipelined data flow graphs**
Hu, Y.; Ghouse, A.; Carlson, B.S.;
Computer Design: VLSI in Computers and Processors, 1993. ICCD '93. Proceedings., 1993 IEEE International Conference on , 3-6 Oct 1993
Page(s): 21 -24

[Abstract] [PDF Full-Text (356 KB)] **IEEE CNF**

Your search matched **1** of **942182** documents.

A maximum of **1** results are displayed, **15** to a page, sorted by **Relevance** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

flexible timing specification in a vhdl synthesis subset

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Flexible timing specification in a VHDL synthesis subset**
Stoll, A.; Biesenack, J.; Rumler, S.;
Design Automation Conference, 1992. EURO-VHDL '92, EURO-DAC '92. European , 7-10 Sep 1992
Page(s): 610 -615

[Abstract] [PDF Full-Text (520 KB)] **IEEE CNF**

Search Results

Search Results for: [scheduling using behavioral templates]
Found 15 of 110,178 searched. > Rerun within the Portal

Search within Results

> Advanced Search > Search Help/Tips

Sort by: **Title** **Publication** **Publication Date** **Score** Binder

Results 1 - 15 of 15 **short listing**

1 Scheduling using behavioral templates pages 101-106 82%
Tai Ly , David Knapp , Ron Miller , Don MacMillen
Proceedings of the 32nd ACM/IEEE conference on Design automation conference ~~January~~ June 1995

2 System partitioning and timing analysis: A strongly polynomial-time algorithm for over-constraint resolution: efficient debugging of timing constraint violations 77%
Ali Dasdan
Proceedings of the tenth international symposium on Hardware/software codesign May 2002
A system of binary linear constraints or difference constraints (SDC) contains a set of variables that are constrained by a set of unary or binary linear inequalities. In such diverse applications as scheduling, interface timing verification, real-time systems, multimedia systems, layout compaction, and constraint satisfaction, SDCs have successfully been used to model systems of both temporal and spatial constraints. Formally, SDCs are modeled by weighted, directed (constraint) graphs. The cons ...

3 Instruction generation for hybrid reconfigurable systems 77%
R. Kastner , A. Kaplan , S. Ogrenci Memik , E. Bozorgzadeh
ACM Transactions on Design Automation of Electronic Systems (TODAES) October 2002
Volume 7 Issue 4
Future computing systems need to balance flexibility,

Jacob, Rebecca (ASRC)

From: STIC-ILL
Sent: Monday, May 12, 2003 11:11 AM
To: Jacob, Rebecca (ASRC)
Subject: FW: ILL order

-----Original Message-----
From: Bates, Darcy
Sent: Monday, May 12, 2003 11:01 AM
To: STIC-ILL
Cc: Harrison, Jeff; Blalock, Derrick (ASRC); Spockhard, Irina (ASRC); Fagbohunka, Bode (ASRC); Thompson, Annette
Subject: ILL order

Hi,

We do not have the following item in STIC. Please order this item for Annette Thompson, CP3-3E06.

ILL Ordering Information

Date Needed<5-14-03>

Art Unit or Location <2825>

Telephone Number <305-7441>

Case # < 09/590,584>

445361

AU: W. Glunz and G. Umbreit
TI: **VHDL for High-Level Synthesis of Digital Systems**
Source: Proceedings of conference as follows from Dialog 165, Eventline:
EVENT TITLE: **1st European Working Conference on VHDL Methods**
EVENT DATE(S): September 4-7, 1990
HOST SITE: Inst. Mediterraneen de Techn.
EVENT CITY: Marseille
EVENT COUNTRY: France
ORGANIZER: Siemens
Petra Michel
A.G. Dept. ZFE ISEAI
Otto Hahn Ring 6
Munich 83 FRG

Note: We have searched for more detailed citation information, this is all we could find.

Thank you,

OCLC - Ø Dialog - Ø
CAS 5/14/03 - NO
BRI Ø
tri doc 5/15

Darcy Bates
EIC 2800 Technical Information Specialist
U.S. Patent & Trademark Office
(703)306-5419 Email: STIC-EIC2800
dbates@uspto.gov